Remarks

Reconsideration of the subject application is respectfully requested.

The claims of the subject application are directed to a digital signal processing apparatus and method in which, *inter alia*, independently reconfigurable processing elements in an array of independently reconfigurable processing elements are configured to perform a block cipher routine.

Figure 3 of the subject application provides an example of an independently reconfigurable processing element. As explained in paragraphs 0017-0019 in the subject application, a reconfigurable cell 200 includes functional units which are activated according to the function being executed by the reconfigurable cell during a processing cycle. The functional units can include, without limitation, a Multiply-and-Accumulate (MAC) functional unit, an arithmetic unit, and a logic unit. The functional units are configured to execute logical operations which include, without limitation, XOR, OR, AND, store, shift, and truncate. Other types of functional units for performing other functions are possible.

In the embodiment of a reconfigurable cell described in Figure 3, the functional units are controlled and activated by a context register. The context register latches a context instruction and provides the context instruction to the appropriate functional unit(s). (*See*, Subject Application, paragraph [0019].)

As a result, routines, such as a block cipher routine, can be executed with the high performance of a hardware implementation such as an ASIC, yet with the flexibility and scalability of software executed by general purpose processors. (*See*, Subject Application, paragraph [0024].)

Claims 1-41 are pending in the Subject Application, with claims 1, 21 and 31 being independent claims.

Official Action – Claim Objections

The Examiner has objected to the claims, noting that "a claim which depends from a dependent claim should not be separated by any claim which does not also

depend from said dependent claim." (Citing, MPEP § 608.01(n), Official Action, p. 2.) Applicants first note that the cited section uses the permissive words "should not" as opposed to the restrictive words "must not." Applicants suggest that, in order to minimize any confusion as to what claims are being referred to in an Official Action or Response, any renumbering of the claims to satisfy MPEP § 608.01(n) be deferred until the Examiner has indicated that Application otherwise is in condition for allowance. By doing so, the same claim numbers will be referenced during the merits examination, and the necessity of cross referencing original and amended claim numbers can be avoided.

Official Action – 35 U.S.C. 102

The Examiner has rejected claims 1-10, 19-25, 30-36 and 41 under 35 U.S.C. 102(e) as being anticipated by US Pat. No. 6,088,800 to Jones et al. (Official Action, p. 2.) Applicants respectfully traverse this rejection.

As understood by Applicants, the Jones et al. reference discloses an architecture of an encryption processor composed of a one-dimensional array of non-reconfigurable autonomous processors. In particular, as disclosed in Fig. 3 and col. 7:15-25 and col. 7:65 to col. 8:6, the Programmable Elements ("PE") in Jones et al. each consist of an ALU operating on words from a register file, which are controlled by a control unit that decodes instructions from a processing element instruction memory. The instruction set of the PE instruction memory is described as "resembling that of a modern RISC processor integer unit." While there is a discussion about enhancements to these instructions that can be executed by these PEs, such as a "modular addition/subtraction instruction," a "modulo adjust instruction," and a "modular multiplication," there is no discussion in Jones et al. about changes to the configuration of the ALUs in the PEs. As understood by Applicants, configuration of each of the PEs, including the ALU, in Jones et al. is the same, although the series of instructions being executed by one PE during a process may be different from the series of instructions being executed by another PE.

In contrast, as illustrated in Figure 3 and described in paragraphs 0017 to 0019 of the subject application, for example, the claimed invention involves configuring

"Independently reconfigurable processing elements." That is, rather than executing instructions from an enhanced instruction set using an ALU of a fixed configuration, such as in Jones et al., the claimed invention in the context of the described embodiment, involves activating or deactivating functional units in a reconfigurable processing element by so that the combination of the activated functional units defines the operation of the reconfigurable processing element as reconfigured for a processing cycle.

While it is the case, as indicated by the Examiner, that a PE in Jones et al. comprises an instruction memory which stores a sequence of instructions for a round of an encryption algorithm, this does not mean that the underlying PE is "reconfigurable." It is the instruction sequence which changes, not the underlying configuration of the PE.

For this reason, it is respectfully submitted that independent claims 1, 21 and 31 of the subject application, which all recite "independently reconfigurable processing elements," are allowable over Jones et al. Further dependent claims 2-20, 22 through 30, and 32-41, which depend from allowable independent claims 1, 21 and 31, are allowable as being dependent from an allowable base claim.

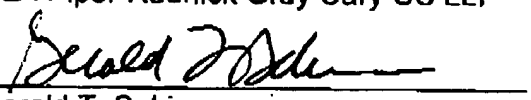
Official Action – 35 U.S.C. 103

The Examiner has rejected claims 11-18, 26-29, and 37-40 under 35 U.S.C. 103(a) as being unpatentable over US Pat. No. 6,088,800 to Jones et al. in view of Sorimachi, US 2002/0181709. (Official Action, p. 4.) The Examiner cites Sorimachi as disclosing an encryption system using a Kasumi algorithm. Applicants respectfully traverse this rejection. As set forth above, Jones et al. do not teach, suggest or make obvious the "independently reconfigurable processing elements" of independent claims 1, 21 and 31. It is respectfully submitted that Sorimachi also does not teach, suggest, or make obvious the "independently reconfigurable processing elements."

Conclusion

For the above reasons it is respectfully submitted that the subject application is in condition for allowance, and the Examiner's indication to that end is respectfully solicited.

Respectfully submitted,
DLA Piper Rudnick Gray Cary US LLP

Dated: August 3, 2005 By: 

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